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CONTACT AND ALIGNMENT MARKER TECHNOLOGY FOR ATOMIC SCALE DEVICE FABRICATION

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This article reports on the technology to link atomic scale structures to macroscopic contact pads. Dedicated processes for electrode pattern formation in several materials have been developed and characterised. For pattern formation in $CoSi_2$ a thermal compromise between proper silicide formation and lateral dimension loss has been established. The thermal stability of Pt and W submicron patterns (or the silicides of these) has been investigated. First results, for W in particular, show that atomically clean and flat surfaces can be realized coexisting with useful metallization patterns.

1. INTRODUCTION

Now that atomic manipulation and other scanning probe microscope (SPM) fabrication techniques are pushing device dimensions down to the molecular scale, dedicated contact technology is required to link the associated ultra-small features to the outside world. Furthermore, SPM manipulation processes require finding and aligning to contact patterns, i.e. require an orientation marker array bridging the macroscopic and microscopic length scales. Besides ranging in details from sub-100 nm to at least 100 microns, the contact pattern should preferably display sub-nm topography and roughness to avoid step coverage problems at the molecular contact. It should also allow for preparation of an atomically clean surface. As DIMES is involved in SPM nanofabrication on Si in ultra-high vacuum (UHV), the electrode and marker material itself should preferably be resistant to the high temperatures, conventionally up to 1200°C, of conventional Si surface preparation. Anticipating electrical measurements at cryogenic temperatures the electrode material should be metallic or even superconducting. Unfortunately, these and other requirements we pose on the metallization are not all fulfilled best by a single material. Different materials perform best for different aspects. In this work we therefore initially explore several materials to see how well they meet the above requirements: $CoSi_2$ because of its promising topography prospects on Si[1] and its superconducting state below 1K; Pt for its chemical inertness and the proven suitability for high resolution contacts to single molecules[2]; and W/WSi_2 for its thermal stability at high temperatures.[3] We will report here mainly on Co and W; Pt, W, and other refractory metals will be discussed in detail in forthcoming work.

2. EXPERIMENTAL

Co, Pt, and W were deposited by e-gun evaporation on Si(111) and Si(100) wafers.

Co surface roughness has been minimised by reducing the deposition rate down to 1-2 Å/s. Co patterns were obtained by evaporation and lift-off, with a PMMA double layer as mask. Exposure was done with an EBPG05 (Leica Cambridge) equipped with a field emission gun operating at 100 kV acceleration voltage. Formation of $CoSi_2$ was achieved by rapid thermal anneal (RTA) in nitrogen ambient. All heating started with a ramp to 500°C in 70 s. From that point heating was either stopped or it was continued at 500°C or with an additional pulse to 700°C. The formation of $CoSi_2$ was checked with HCl/H_2O_2 treatment which removes Co and monosilicides, and subsequent Auger surface analysis.

Tungsten was also patterned by evaporation and lift-off, but in this case with a stack of silicondioxide and low stress siliconnitride as the lift-off mask, and 50 nm PMMA 950K on top of this for the pattern definition. Pattern transfer from PMMA to nitride was by dry etching in a SF_6/He plasma, followed by a wet underetch of the oxide with buffered HF. After W deposition (at a rate of

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several Å/s) lift-off was performed in HF solution. The important advantage of the above scheme is the potentially very clean surface (no organic contaminants) existing after liftoff, while the surface will also be hydrogen-terminated, hence mostly oxygen-free. This clean surface is important especially in the case of W, which when evaporated tends to change part of the organic resist into a carbon contamination which is hard to remove. The hydrogen-termination is important for cleaning in UHV since very thin or incomplete silicon oxides can be more easily removed at relatively low temperature.[4]

Platinum was deposited on top of a thin Ti layer for good attachment to the surface. Both inorganic and organic masks were used, according to the same procedures as described above.

Sample inspection was done with AFM (PSI Autoprobe M5), and SEM (Hitachi S900). The Pt and W patterns were also investigated in a UHV system with scanning tunneling microscopes (Omicron VT-STM) and sample preparation stages.

The samples introduced in the UHV system were cleaned by thermal anneal only, or by an *in situ* hydrogen plasma treatment[5] at 450°C, followed by thermal anneal at temperatures between 700°C and 1250°C. They were subsequently investigated in the STM. We are investigating additional wet cleaning procedures to improve on the cleanliness of, in particular, the patterns created with organic masks. Recent work by Dunn et al. describes reasonable cleanliness for a surface with Ta patterns cleaned with commercial resist stripper.[6]

3. RESULTS AND DISCUSSION

Cobalt/Cobalt silicide:

The AFM images in figure 1 show a 5 nm thick Co film on Si(111) before (a) and after (b) RTA ramp to 500°C and after subsequent HCl/H_2O_2 treatment (c). The rms roughness of the untreated Co film is in the 0.2 nm range, increasing to 4.22 nm after the anneal. After removal of unreacted or partly reacted material in the HCl/H_2O_2 step rms roughness drops to 0.3 nm. In this way we investigated a range of thermal treatments. The results are collected in table 1

Further anneal at 500°C creates after about 90 seconds a completely reacted film with a rms roughness of 1.57 nm. Prolonged heating at 500°C deteriorates the film quality, apparently by a combined clustering and diffusion process. When after the ramp an additional heat pulse to 700°C is applied $CoSi_2$ formation is clearly enhanced given the rms values before and after wet treatment. Up to about 90s the final result is comparable to the 500°C treatment.

Table 1 Roughness of Co films before and after RTA and wet ech treatment

RTA Process*	time (s)	rms (nm)	after wet etch (nm)
-	-	0.196	-
ramp	-	4.22	0.30
ramp + 500	30	4.03	0.29
ramp + 500	90	1.57	1.57
ramp + 500	300	6.35	900.-
ramp + 700	30	1.84	3.27
ramp + 700	60	1.52	2.28
ramp + 700	90	4.53	1.57
ramp + 700	300	4.96	280.-

*ramp = linear heating to 500°C in 70 seconds

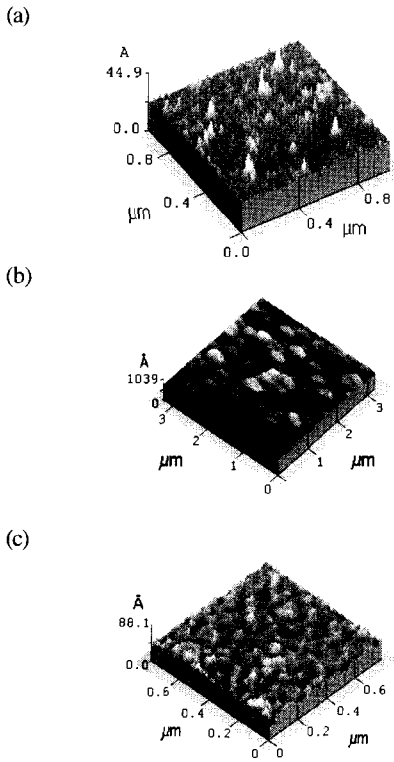

Figure 1. AFM scan of Co film after various stages of film treatment for $CoSi_2$ formation.

Prolonged heating seriously deteriorates. The somewhat increased roughening at 700°C happens probably because $CoSi_2$ species start to agglomerate.[7] Altogether it makes clear that $CoSi_2$ is a less useful electrode material where an additional high temperature (>= 500°C) cleaning anneal of the Si surface is needed. An alternative room temperature treatment to get a clean H-terminated Si surface would be in mixed HCl/HF solutions[8].

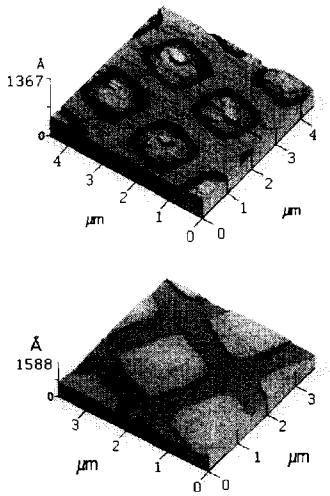

Figure 2. Co dot pattern sintered with additional pulse at 700°C for 30 s (top) and 90 s (bottom)

We made patterns of 1 x 1 μm^2 Co dots by lift-off and investigated the solid state reaction and dimension control during the various treatments. For a treatment of 60 s at 500°C before the wet etch the reacted Co dots don't show noticeable lateral diffusion. After removal of all residues by the wet treatment it is clear that at the center $CoSi_2$ is formed while at the edges monosilicide dominates. Silicidation creates unwanted trenches of tens of nanometers deep. Moreover the solid state reaction induced sub-surface dimension loss of 150 nm at each side. Shorter time at 500°C just yields a hole after the wet step. Thus, merely monosilicide was formed. Prolonged treatment at 500°C shows how solid state reaction continued sub-surface and dimension control is severely lost. Additional pulsing to 700°C sharply promotes the $CoSi_2$ formation and trenching around the edges decreases, however at the cost of lateral dimension control. For an additional heat pulse of 90 seconds at 700°C trenching disappeared, but lateral offset of $Si/CoSi_2$ boundaries is approximately 220 nm. See figure 2.

Platinum/Platinum silicide:

Both Pt and W films were evaporated to approximately 10 nm thickness. Film quality (absence of granularity) appeared to be very good in electron micrographs and STM images. We therefore expect that the thickness can be further reduced without problems. Resolution down to 50 nm is relatively straightforward to obtain.

We have created Pt contact patterns on hydrogen-terminated Si(100) surface, and imaged those by UHV-STM. We have, so far, not obtained atomic resolution on such surfaces. The procedures for advanced wet cleaning and hydrogen passivation are well-developed, however, and we expect it will be possible to obtain surfaces with high quality terraces and low defect-density.[9] Heating to 1250°C for 1 minute destroys most of a Pt pattern. We have not yet investigated the lower temperature cleaning described below for W.

Tungsten/Tungsten silicide:

Figure 3 shows a W metallization pattern after annealing at 1250°C. The high temperature causes large, unconnected, WSi_2 grains to form. Although the melting point of WSi_2 is the highest known to us (2165°C) even in this material the diffusion of the constituent elements is too large at 1250°C.

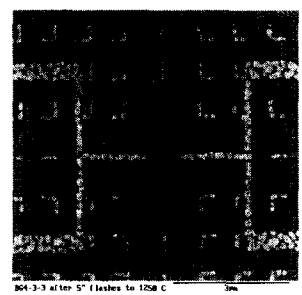

Figure 3. W metallization after 25" 1250°C anneal.

From images such as these, a 1000°C anneal would appear already acceptable. Such a high temperature, however, has the risk of strong trench-formation around the metallization (at least for (100) surfaces). Part of the Si is consumed for silicidation of the W, and we often find trenches with surfaces approximating the stable (111) plane. An even lower processing temperature and/or films thinner than the present 10 nm may therefore be necessary.

We have annealed W metallization at 750°C after cleaning by atomic hydrogen. This temperature let the metal pattern largely intact, and showed Si terraces, in some cases extending all the way to the base of the metallization (fig. 4). When zooming in, these terraces show atomic resolution. Some trench formation was observed in this case, so that an even lower temperature might be preferred. We encountered problems with organic contamination (resulting in carbide crystals on the final surface) on this sample, but expect that this can be avoided by cleaner processing and perhaps additional wet cleaning steps.

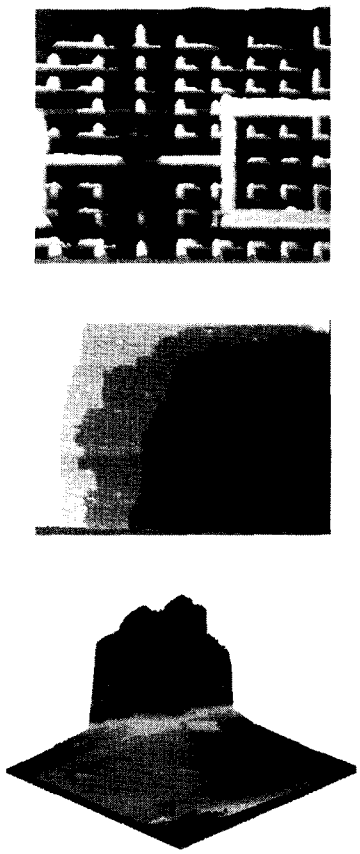

Figure 4. W metallization after 30' 750°C. STM 7 micron overview (top): approx. 100nm scans with details of Si surface (middle) and connection to metal marker (bottom, terraces visible).

4. CONCLUSIONS

Compromise between $CoSi_2$ formation and minimal lateral diffusion results in thermal treatment at 700°c for 90 seconds. It is not clear yet whether such a process allows for atomically clean and flat surfaces between the metallization.

Thin films of high melting point metals which form high melting point silicides (e.g. Pt and W) show good results. Apart from the relatively strong topography (the metallization is nm's higher than the silicon surface) patterning and cleaning are possible with high accuracy. We are aiming at applying metals that combine the robustness of W or Pt, and the flat topography associated with Co.

Minimization of trench formation around the metallization is important. This can probably be obtained by using the lowest possible temperatures, perhaps avoiding silicidation altogether.

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